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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
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EXAMINER	
DHARIA, R	
ART UNIT	**PAPER NUMBER**
2305	5

DATE MAILED: 10/16/97

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☑ Responsive to communication(s) filed on 6/30/97.

☑ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire _____ month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1 - 74 is/are pending in the application.

Of the above, claim(s) 4, 7, 8, 10, 12, 22 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-3, 5, 6, 9, 11, 13-21, 23-35, 37-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, 69-73 is/are rejected.

☒ Claim(s) 36, 40, 44, 48, 52, 56, 60, 64, 68, 74 is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

– SEE OFFICE ACTION ON THE FOLLOWING PAGES –

* U.S. GPO: 1996-409-290/40029

Part III DETAILED ACTION

Claim Objections

1. Claims 36, 40, 44, 48, 52, 56, 60, 64, 68, and 74 are objected to because of the following informalities: The above listed claims are all dependent upon canceled claim 10. Appropriate correction is required.

2. On page 9 of the amendment, claim 69 was listed twice as a typographical error. The second occurrence of the claim has been deleted.

Claim Rejections - 35 USC § 112

3. Claims 30 and 31 have been amended by the amendment and therefore the rejection is withdrawn.

Claim Rejections - 35 USC § 101

4. Claim 12 has been canceled by the amendment and therefore the rejection is withdrawn.

Double Patenting

5. Claims 4, 7, and 10 have been canceled by the amendment and therefore the double patenting rejection has been withdrawn.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

7. Claims 1-3, 5-6, 9, 11, 32-35, 37-39, 41-43, 45-47, 49-51, 53-55, 57-59, 61-63, 65-67, and 71-73 are rejected under 35 U.S.C. § 103 as being unpatentable over Hollowell, II et al. in view of Kikinis.

As per claims 1, 2, 3, 9, and 32, Hollowell discloses the claimed invention including a provision for user input (Fig. 1); a provision for output (Fig. 1); a CPU coupled to the input and output (Fig. 1; col. 4, lines 6-7); the input is a keyboard (Fig. 1; col. 4, lines 42-44); the output is a display device (Fig. 1; col. 4, lines 21-22); a temperature level detector (Fig. 1; col. 4, lines 47-48); and a thermal management system that stops the power to the CPU when the temperature detected exceeds a reference temperature (Abstract; Fig. 2). However, Hollowell does not teach stopping the clock signals when a detected temperature rises above a reference temperature level. Kikinis teaches a system for controlling temperature buildup in an IC which

employs a temperature sensor to provide an indication of the IC temperature to a control circuit which is configured to adjust the clock speed based upon a function of the temperature of the IC or its package (Abstract). Further, Kikinis teaches that it is known to selectively stop clock signals when the detected temperature rises above a reference temperature level (Abstract; Fig. 3, 6). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the selectively stopping the clock signals based upon rising temperatures exceeding a reference temperature as taught by Kikinis, to monitor the temperature levels in the computer, to prevent excessive temperature which may damage vital components or circuitry.

As per claims 5 and 11, Hollowell and Kikinis disclose the claimed invention as above in claims 1-3. However, Hollowell does not teach a monitor stopping the clock signals to the CPU only when the CPU is processing non-critical I/O. Kikinis teaches that it is known to include stop the clock to the CPU when it is processing non-critical I/O (col. 5, lines 10-22). It would have been obvious to one having ordinary skill in the art at the time the invention was made to stop the clock only when the CPU is processing non-critical I/O as taught by Kikinis, to prevent losing any vital information or processing that may occur during an I/O operation.

As per claim 6, Hollowell and Kikinis disclose the claimed invention as above in claims 1-3. However, Hollowell does not teach a CPU receiving a one of a first clock signal at a first speed or a second clock signal at a second speed and the CPU receives the first clock signal when the temperature is below the reference temperature and the receives the second clock signal when the temperature is greater than or equal to the reference temperature. Kikinis teaches that it is

known to provide first and second clock signals with first and second speeds to the CPU (col. 4, lines 23-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Kikinis, to provide different clock speeds based upon the required load of the CPU.

As per claims 33-35 and 37-39, Hollowell and Kikinis disclose the claimed invention as described above. However, Hollowell does not teach the monitor is on board the CPU and the monitor detects via a temperature sensor. Kikinis teaches that it is known to have a monitor on the board with the CPU and the monitor detects via a temperature sensor (Fig. 2, 3; col. 3, lines 8-10). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the above features as taught by Kikinis, to provide an accurate and efficient way to measure temperature.

As per claims 41-43, 45-47, and 49-51, Hollowell and Kikinis disclose the claimed invention as described above. Furthermore, Hollowell and Kikinis teach that the temperature sensor is located on the CPU board (Fig. 1) or on the CPU (Fig. 3). The location of the temperature sensor is dependent upon the area of concern. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to locate the temperature sensor as taught by Hollowell and Kikinis to provide the system designer the freedom to measure in close proximity to area of temperature concern.

As per claim 53-55, Hollowell and Kikinis disclose the claimed invention as described above. Furthermore, Hollowell teaches the temperature sensing device may be a thermistor (col. 6, lines 31-33).

As per claim 57-59, Hollowell and Kikinis disclose the claimed invention as described above. Furthermore, Hollowell teaches the temperature sensing is monitored periodically (col. 6, lines 46-47).

As per claim 61-63, Hollowell and Kikinis disclose the claimed invention as described above. Furthermore, Hollowell teaches the frequency of temperature sensing changes as the temperature reaches a preselected threshold value (col. 7, lines 44-50).

As per claim 65-67, Hollowell and Kikinis disclose the claimed invention as described above. However, Hollowell does not teach that the temperature sensing is user modifiable. Kikinis teaches that it is known for the temperature sensing to be user modifiable (col. 5, lines 64-66). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the user modifiable temperature sensing as taught by Kikinis to give the user the flexibility to adjust the temperature sensing for testing purposes.

As per claim 71-73, Hollowell and Kikinis disclose the claimed invention as described above. However, Hollowell does not teach the monitor uses a control system of continuous feedback loops. Kikinis teaches that it is known to use a control system of continuous feedback loops (Fig. 3). It would have been obvious to one of ordinary skill in the art at the time of the invention to include the continuous feedback loops as taught by Kikinis, to maintain and regulate

the temperature in the IC to prevent large temperature swings which causes excess power and could cause physical damage to the components.

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollowell, II et al in view of Kikinis and further in view of Smith et al.

As per claim 13 and 16, Hollowell and Kikinis disclose the claimed invention, including the temperature level detector, a CPU, and the CPU is part of a computer (Fig. 1; col. 4, lines 3-7). However, Hollowell and Kikinis do not teach activating a hardware selector based upon determining if the CPU may rest. Smith et al. teaches that it is known to activate a hardware selector based upon determining if the CPU may rest (Abstract; col. 7, lines 49-54). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Smith, since logic is needed to provide the appropriate clock speeds to the CPU based upon each condition.

As per claim 14, Hollowell, Kikinis, and Smith disclose the claimed invention as in claim 13 above. However, Hollowell and Kikinis do not teach the hardware selector applies oscillations to the clock input of the CPU based upon if the CPU is to sleep/rest or if the CPU is active. Smith teaches that it is known to have the hardware selector apply oscillations to the clock input of the CPU based upon the CPU state (Abstract; col. 8, lines 9-13; col. 8, lines 18-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Smith, since the CPU requires different clock speeds based upon

the state of the CPU. A first clock speed is slow if the CPU is in a rest or sleep mode and a second clock speed is fast if the CPU requires activity.

As per claim 15, Hollowell, Kikinis, and Smith discloses the claimed invention as in claim 13 above. However, Hollowell and Kikinis do not teach the hardware selector preventing the oscillations for the clock input to the CPU if the CPU is to rest or supplies oscillations to the CPU at full speed if the CPU is to be active. Smith teaches that it is known to provide full speed to the CPU when it is active and not when it is in sleep/rest mode (Abstract; col. 8, lines 9-13; col. 8, lines 18-53). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Smith, since the CPU requires different clock speeds based upon the state of the CPU. A first clock speed is slow if the CPU is in a rest or sleep mode and a second clock speed is fast if the CPU requires activity.

9. Claims 17-21, 23-29, and 69-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollowell, II et al in view of Kikinis and further in view of Kenny et al.

As per claims 17, 18 and 21, Hollowell and Kikinis disclose the claimed invention including monitoring temperature levels in a computer. However, Hollowell and Kikinis do not teach predicting activity and temperature levels relevant to the operation of a CPU within the computer and using the predictions for automatic temperature control. Kenny teaches that it is known to predict activity levels within a computer and using the prediction for automatic control and also, remain transparent to the user (col. 1, lines 51-64). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught

by Kenny, since having the capability to predict temperature rises and automatically control them, prior to the occurrence could prevent premature failure of the CPU or circuit components.

As per claims 19, 20, and 23, Hollowell and Kikinis teach the disclosed invention as claims 17, 18, and 23 above. However, Hollowell and Kikinis do not teach user modification of automatic activity and temperature level predictions and using modified predictions for automatic temperature control. Kenny teaches that it is known to allow user modification of automatic activity level predictions and using the modified predictions for automatic control (col. 2, lines 48-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to include the above as taught by Kenny, since allowing the user to modify temperature levels would allow for different manufacturer's components that have various temperature specifications.

As per claims 24-29, Hollowell, Kikinis and Kenny discloses the claimed invention as described in the claims above. Hollowell, Kikinis and Kenny teach a CPU coupled to a clock (Fig. 1) and a monitoring temperature levels within the computer system (Abstract). Further, Hollowell, Kikinis and Kenny teach regulating the clock speed based upon the temperature fluctuations in the IC or its package, as per the claims above. Also, Hollowell, Kikinis, and Kenny teach that the clock speed is inversely proportional to the temperature of the IC and thus inherently teach that at maximum temperature the clock speed would be minimum.

As per claims 69 and 70, Hollowell, Kikinis and Kenny discloses the claimed invention as described in the claims above. However, Hollowell and Kikinis do not teach the temperature

levels are predicted using the temperature prediction mode and without using temperature sensors. Kenny teaches that it is known to use the above features (col. 1, lines 51-67; col. 2, lines 1-2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the above features as taught by Kenny, to prevent premature failure of the CPU or circuit components.

10. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hollowell, II et al in view of Kikinis and further in view of Gephardt et al.

As per claims 30 and 31, Hollowell and Kikinis disclose the claimed invention as described in the above claims. However, Hollowell and Kikinis do not teach the clock manager stops clock signals from being sent to a PCI bus coupled to the CPU or any other CPUs coupled to the PCI bus. Gephardt teaches that the above features are well known (Fig. 2, col. 11, lines 13-21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the above features, as taught by Gephardt to more efficiently conserve power by managing power also to external devices.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rupal Dharia whose telephone number is (703) 305-4003. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey, can be reached on (703) 305-9705. The fax phone number for this Group is (703) 308-5356.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**jack.harvey@uspto.gov**].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express

waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

JACK B. HARVEY
SUPERVISORY PATENT EXAMINER
GROUP 2300

RDD

October 8, 1997